**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| In re Patent of: Kenneth Martin Jacobs | Group Art Unit: 3992 |
| Appl. No.: 15/217,612 | Examiner: HUGHES, DEANDRA M |
| Filed: Jul 22, 2016 | Confirmation No: 5884 |
| U.S. Patent No. 9,699,444<br>Issue Date: July 4, 2017<br>**Reexamination Control No. 90/015,245** | Atty. Dkt. No.: 20311.0001.REEX00 |
| Title: FASTER STATE TRANSITIONING FOR CONTINUOUS ADJUSTABLE 3DEEPS FILTER SPECTACLES USING MULTI-LAYERED VARIABLE TNT MATERALS | |

Mail Stop "Ex Parte Reexam"
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# RESPONSE TO FINAL OFFICE ACTION OF APRIL 19, 2024

Enclosed herewith is VDPP, LLC's Response pursuant to 37 C.F.R § 1.111 and 1.550 to the Final Office Action issued on April 19, 2024.

## TABLE OF CONTENTS

## Patent Owner's Exhibits

| Exhibit No. | Description |
|---|---|
| 2004 | PRINCIPLES OF COMPUTER ARCHITECTURE |
| 2005 | LM1881 Video Sync Separator |
| 2006 | MM5483 Liquid Crystal Display Driver |
| 2007 | Microprocessor vs. Integrated Circuit--What's the Difference?<br><br>Source: https://resources.pcb.cadence.com/blog/2020-microprocessor-vs-integrated-circuit-what-s-the-difference |

## I. STATUS OF THE CLAIMS

Claims 1-27 stand issued in U.S. Patent No. 9,699,444 ("the '444 Patent") of which claims 1, 26 and 27 are subject to reexamination. Claims 2-25 are not subject to reexamination. Of those claims subject to reexamination, claims 26 and 27 are rejected, claim 1 is confirmed patentable. The Patent Owner has not presently amended the claims.

## II. OVERVIEW OF THE OFFICE ACTION

In the Final Office Action in Ex Part Reexamination issued on April 19, 2024 ("FOA"), the Examiner rejects claims 26 and 27 on the following grounds:

Claims 26 and 27 are rejected under 35 U.S.C.§ 102(b) as being anticipated by Okamura (U.S. 6,061,103).

Patent Owner disagrees with Examiner's assessment. Patent Owner respectfully traverses the ground of rejection and requests entry of the present Response and Reconsideration of the rejection in view of the arguments presented herein.

## III. CLAIM REJECTION

### A. Okamura Fails to anticipate Claims 26 and 27

The Office action rejects Claims 26 and 27 under 35 U.S.C.§ 102(b) as being anticipated by Okamura. Patent Owner respectfully submits that Okamura fails to

teach or suggest each and every limitation of Claims 26 and 27 and requests that the rejection of Claims 26 and 27 be withdrawn.

### 1. Claim 26

The Requester has divided claim 26 into elements for consideration as follows:

[26-Preamble] An apparatus comprising:

[26a] a storage adapted to: store one or more image frames; and

[26b] a processor adapted to: obtain a first image frame from a first video stream;

[26c] generate a modified image frame by performing at least one of expanding the first image frame, shrinking the first image frame, removing a portion of the first image frame, stitching together the first image frame with a second image frame, inserting a selected image into the first image frame, and reshaping the first image frame, wherein the modified image frame is different from the first image frame;

[26d] generate a bridge frame, wherein the bridge frame is a solid color, wherein the bridge frame is different from the first image frame and different from the modified image frame;

[26e] display the modified image frame; and display the bridge frame.

#### a. Element [26b]

Okamura does not disclose Element [26b], particularly, Okamura does not disclose "processor."

Regarding the limitation “processor,” the FOA states that:

Examiners agree the following is the ordinary and customary meaning of "processor," (i.e., "central processing unit') because Examiners do not find that PO has clearly set forth an explicit definition of "processor' in the '444 Patent or that PO has used expressions of manifest exclusion or restriction during prosecution of the '444 Patent. FOA, 4-5.

PO incorporates the above definition of "instruction' into the Microsoft Dictionary's Definition of" CPU' and argues the processor disclosed at figure 39 of Okamura does not fall within the scope of this definition because: (1) the synchronous separator circuit (#111) of figure 39 is a circuit structure, not a processor; and (2) the circuit structure in Okamura has no ability to interpret and execute instructions. FOA, 5-6.

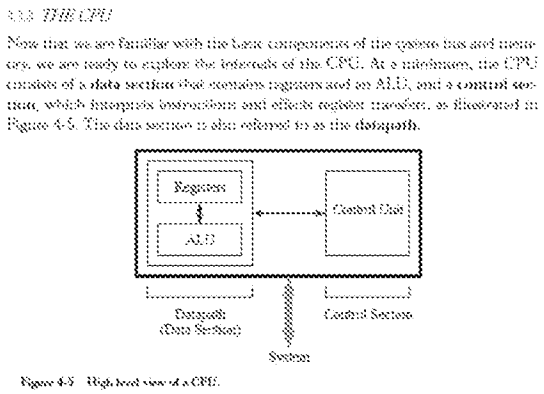
As to (1), Examiners are not persuaded that the synchronous separator circuit (#111) of figure 39 is not a "processor," within the ordinary and customary meaning of this term, because the Microsoft Computer Dictionary definition states that "early minicomputers contained circuit boards full of integrated circuits that implemented the CPU." Moreover, it is well-known to one of ordinary skill in the art that a processor/CPU is merely an integrated circuit. Because Examiners find the circuit disclosed at figure 39 of Okamura is merely a representation of the circuit found in

the processor, Examiners disagree that figure 39 is not a "processor' within the ordinary and customary meaning of this term. FOA, 6.

As to (2), Examiners are not persuaded that the processor disclosed at figure 39 of Okamura has no ability to interpret and execute instructions because, e.g., the sampling timing signals and the control signals of sampling control circuit (#117L) are instructions in that they instruct the liquid control circuit (#118L) and the switch circuit #114R) (see col.24:4-23). FOA, 6-7.

As to (1), PO cannot agree that "the circuit disclosed at figure 39 of Okamura is merely a representation of the circuit found in the processor."

Referring to Fig.4.5(reproduced below) of Principles of Computer Architecture, a CPU (processor) includes three kinds of circuits: registers, ALU and control unit. Ex2004, 110.




Ex2004, Figure 4-5

The **control unit of a computer is responsible for executing the program instructions, which are stored in the main memory**. Ex2004, 110. The ALU

implements a variety of binary (two-operand) and unary (one-operand) operations. Examples include add, and, not, or, and multiply. Operations and operands to be used during the operations are selected by the Control Unit. Ex2004, 112. That is, the control unit of a computer is a universal controller to perform kinds of different operations based on program instructions stored in the main memory.

Figure 39 (reproduced below) of Okamura does not include a representation of the circuit found in the processor.

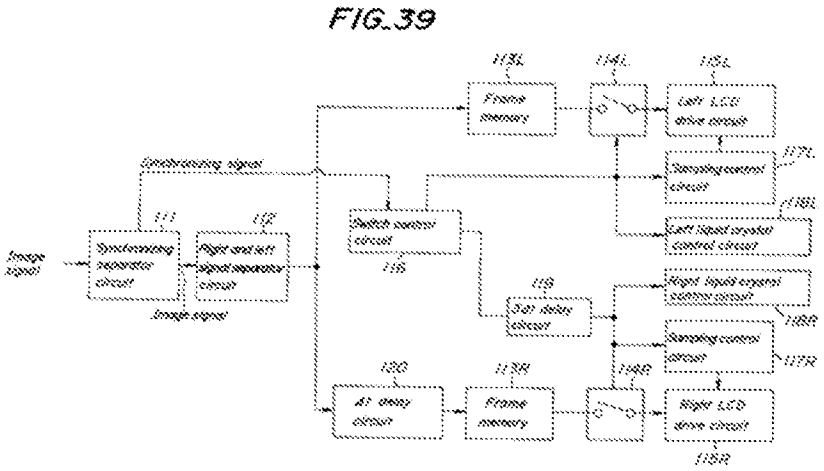
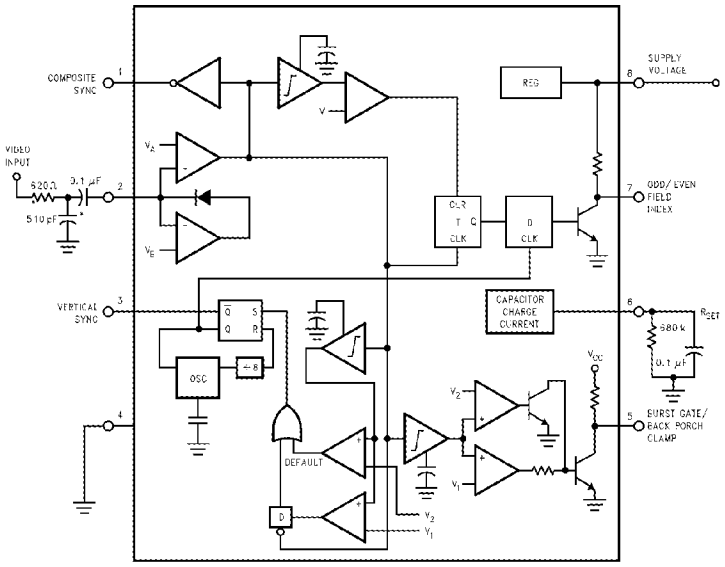



**Fig. 39 - Okamura**

For example, Okamura does not disclose a specific circuit of the synchronous separator circuit (#111) of figure 39, and Examiners are not persuaded that the synchronous separator is not a "processor." Texas Instruments provides a specific circuit (LM1881) of a typical synchronous separator as follower (Ex2005, 6):




**Functional Block Diagram of LM1881**

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5 V (p-p) to 2 V (p-p) can be accommodated. (Ex2005, 6)

The cited portion of LM1881 shows that a typical synchronous separator circuit is a dedicated digital-analog mixed signal integrate circuit (IC) to strip the synchronization signals from composite video sources. It does not relate to registers, ALU and control unit of a processor, that is, it is not a "processor."

Another example is LCD driver circuit (#115) of figure 39, Okamura does not disclose a specific circuit of the LCD driver circuit, Texas Instruments provides a specific circuit (MM5483) of a typical synchronous separator as follower (Ex2006, 1):

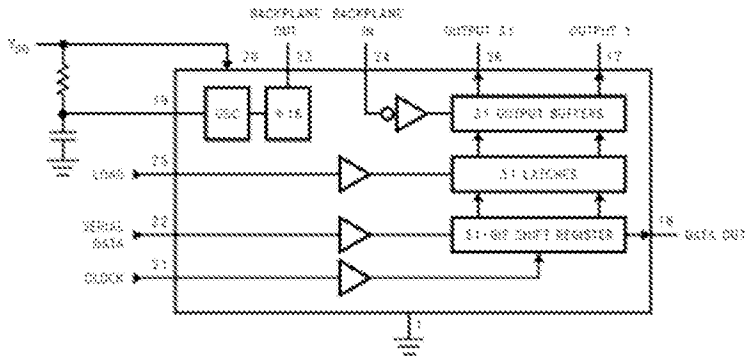


Figure 1. MM5483 Block Diagram

**Functional Block Diagram of MM5483**

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received. Ex2006, 1.

The cited portion of LM1881 shows that a typical LCD driver is a dedicated IC to drive LCD display, a load pulse is used to control the data input, it is not necessary to use a computer to control LM1881, a digital circuit which has ability to output load pulse can be employed to control LM1881.

As to (2), Examiners content that the sampling control circuit (#117) can generate sampling timing signals and control signals to instruct the liquid control circuit (#118L), such that circuit disclosed at figure 39 of Okamura has ability to interpret and execute instructions.

Patent Owner respectively submits that the sampling control circuit (#117) is a delicate control circuit to control liquid control circuit (#118), it includes combinational circuits and sequential circuits which can generate timing sequence

signals to control (instruct) liquid control circuit (#118), which means the sampling control circuit (#117) can generate a delicate instruction to instruct liquid control circuit (#118), but the sampling control circuit (#117) cannot receive different instructions from memory of a computer and interprets the instructions and executes different instructions just like the control unit of a processor which is a universal controller to perform kinds of different operations based on program instructions stored in the main memory of a computer. Therefore, the circuit disclosed at figure 39 of Okamura has no ability to interpret and execute instructions.

Examiners also content the Microsoft Computer Dictionary definition states that "early minicomputers contained circuit boards full of integrated circuits that implemented the CPU." It is well-known to one of ordinary skill in the art that a processor/CPU is merely an integrated circuit. FOA, 6.

The context of Microsoft Computer Dictionary definition states that "early minicomputers contained circuit boards full of integrated circuits that implemented the CPU. Single-chip central processing units, called microprocessors, made possible personal computers and workstations." Ex3003. thus "early minicomputers contained circuit boards full of integrated circuits that implemented the CPU" means early minicomputers include a plurality of circuit boards and not integrated into a single chip. Patent Owner appreciates that a processor/CPU is an integrated circuit. "A microprocessor is an integrated circuit, but not all integrated circuits are

microprocessors." (Ex2007, 2). Unlike other integrated circuits, a microprocessor functions as a computing brain. It is able to process logical and arithmetic instructions that are programmed into it. A microprocessor consists of an arithmetical and logic unit (ALU), a control unit, and a register array. (Ex2007, 3).

The circuit disclosed at figure 39 of Okamura has no ability to interpret and execute instructions, although it includes kinds of dedicated integrated circuits to display image, it is not a processor.

Examiners further content that: Okamura necessarily discloses a "processor" because the pixel shifts of figure 36 are necessarily images processed by a computer. Specifically, it is well-known that a pixel is the smallest unit of a digital image. Because pixels are the basic logical unit in digital graphics, they are necessarily processed by a computer.

Patent Owner respectively submits that complicated image operation does require a "processor" to process, but simple image operations (such as image display) are not necessarily processed by a "processor." Pixels are the basic unit in digital graphics, they can be processed by a digital circuit which is not necessarily a computer.

Specifically, regarding figure 36 (Reproduced below), Okamura depicts as follow:

FIG. 36 shows the change of the images on the display element in this embodiment. As shown in FIG. 36, at an instant (time) t1, a picture 1 is displayed on the display element, at a time t2, the picture 1 is gradually rewritten by a black image from upper side and at a time t3, the picture 1 is wholly replaced by a black image. At this instant, the pixel shifting is performed, at a time t4, the black image is gradually rewritten by a picture 2 from upper side, and at a time t5, whole image of picture 2 is displayed. If such an operation is performed, the instant in which the picture 1 and the picture 2 are displayed simultaneously, is not present, the pixel shifting can be performed by wholly separating the pictures 1 and the picture 2, so that the resolution can be increased. Okamura, 22:57-23:3.

FIG. 36

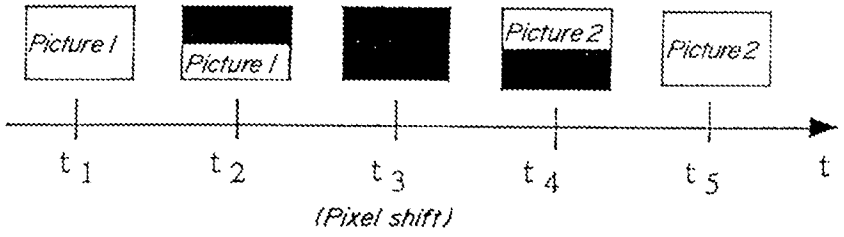



**FIG. 36 - Okamura**

Picture 1 and picture 2 can be displayed on the display element using the circuit structure disclosed in Figure 39 of Okamura, picture 1 is gradually rewritten by a black image can be performed by a point-by-point scanning circuit (which is well-known in the art), Since circuit structure disclosed in Figure 39 and point-by-

point scanning circuit are not "processor," the pixel shifts of figure 36 are not necessarily images processed by a computer.

Regarding the term "computer," Okamura only discloses:

In FIG. 32, the display apparatus unit 81 is connected to a conventional video deck and a TV tuner through the cable 88 to display the image or to a computer to display the image of a computer graphics and a message image from the computer. Alternatively, the display apparatus unit 81 is provided with an antenna without using the cable 88, to receive the image signals externally as an electromagnetic wave. Okamura, 21:65 -22:5.

The cited portion of Okamura shows "computer" is employed to send image signal to display apparatus unit 81, the "computer" does not perform the operations in the elements [26b]-[26e] in claim 26, there are performed by circuit structure disclosed in Figure 39 of Okamura.

Regarding the limitation, the "444 patent use a processor to process image stored in a memory (the storage of element [26a]), processing the image includes "generate a modified image frame by performing at least one of expanding the first image frame, shrinking the first image frame, removing a portion of the first image frame, stitching together the first image frame with a second image frame, inserting a selected image into the first image frame, and reshaping the first image frame" of element [26c], the image in the memory is modified by the processor, the modified

image is stored in the memory and then the processor output the modified image to the display.

On the contrary, Okamura's computer only output the image to the display on a display element, and then circuit structure (such as a point-by-point scanning circuit) disclosed in Figure 39 gradually rewritten the displayed image by a black image from upper side such that removing a portion of the first image frame. Okamura, 22:57-23:3. That is "removing a portion of the first image frame" is performed by a point-by-point scanning circuit, not by a processor.

Therefore, Okamura does not disclose "processor" as required by claim 26, claim 26 is not anticipated by Okamura, since "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051,1053 (Fed. Cir. 1987).

**2.Claim 27**

Claim 27 depends from claim 26 and is not anticipated by Okamura for at least the same reasons.

## IV. CONCLUSION

Therefore, the Examiner should find that claims 26 and 27 are patentable over the prior art.

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