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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/015,245	06/05/2023	9699444	20311.0001.REEX00	5884

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EXAMINER
HUGHES, DEANDRA M

ART UNIT	PAPER NUMBER
3992	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/015,245* .

PATENT UNDER REEXAMINATION *9699444* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Ex Parte Reexamination Advisory Action ***Before the Filing of an Appeal Brief***	**Control No.** 90/015,245	**Patent Under Reexamination** 9699444	
	Examiner DEANDRA M HUGHES	**Art Unit** 3992	**AIA (FITF) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

THE PROPOSED RESPONSE FILED 19 June 2024 FAILS TO OVERCOME ALL OF THE REJECTIONS IN THE FINAL REJECTION MAILED 19 April 2024.

1. ☑ Unless a timely appeal is filed, or other appropriate action by the patent owner is taken to overcome all of the outstanding rejection(s), this prosecution of the present *ex parte* reexamination proceeding WILL BE TERMINATED and a Notice of Intent to Issue *Ex Parte* Reexamination Certificate will be mailed in due course. Any finally rejected claims, or claims objected to, will be CANCELLED.
   THE PERIOD FOR RESPONSE IS EXTENDED TO RUN 5 MONTHS FROM THE MAILING DATE OF THE FINAL REJECTION.
   Extensions of time are governed by 37 CFR 1.550(c).

NOTICE OF APPEAL

2. ☐ An Appeal Brief is due two months from the date of the Notice of Appeal filed on _____ to avoid dismissal of the appeal. See 37 CFR 41.37(a). Extensions of time are governed by 37 CFR 1.550(c). See 37 CFR 41.37(e) .

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final action, but prior to the date of filing a brief, will not be entered because:
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the proceeding in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____ (See 37 CFR 1.116 and 41.33(a)).
4. ☐ Patent owner's proposed response filed _____ has overcome the following rejection(s): _____
5. ☐ The proposed new or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
6. ☐ For purposes of appeal, the proposed amendment(s) a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claim(s) would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) patentable and/or confirmed: _____
   Claim(s) objected to: _____
   Claim(s) rejected: _____
   Claim(s) not subject to reexamination: _____

AFFIDAVIT OR OTHER EVIDENCE

7. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____ .
8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because patent owner failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence fails to overcome all rejections under appeal and/or appellant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☑ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☑ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: SEE ATTACHMENT .
12. ☐ Note the attached Information Disclosure Statement(s), PTO/SB/08, Paper No(s) _____ .
13. ☐ Other: See Continuation Sheet .

/DEANDRA M HUGHES/ Reexamination Specialist, Art Unit 399	/CHRISTINA Y. LEUNG/ Primary Examiner, Art Unit 3991	

cc: Requester (if third party requester)

Continuation of REQUEST FOR RECONSIDERATION/OTHER 13. Other:

As to Item (10), which requires an explanation of the status of the claims after entry of the other evidence, claims 26-27 are rejected.

As to Item (12), Examiners provide the PTO-892 merely to cite the references provided in the remarks. "The Microprocessor vs. Integrated Circuit—What's the difference" is not cited because a publication date has not been provided.

Ex Parte Reexamination Advisory Action Attachment

The claim limitation at issue in this advisory action is *"...a processor adapted to...generate a modified image by performing at least one of removing a portion of the 1st image frame...."* Specifically, Patent Owner ("PO") argues that Okamura does not anticipate claims 26 and 27 because figure 39 of Okamura, which was cited as reading on the claimed "*processor*," is not a "*processor*" within the ordinary and customary meaning of the term. Thus, the crux of the issue is the scope of the ordinary and customary meaning of the term "*processor*."

In these remarks, PO argues Okamura's figure 39 does not read on the claimed "*processor*" because the ordinary and customary meaning of the term "*processor*" necessarily includes registers, an ALU, and a control unit, as shown in Figure 4-5 of a textbook titled Principles of Computer Architecture published August 1999.

In the final action, Examiners agreed that the ordinary and customary meaning of the claim term "*processor*" is the definition for a "CPU" provided by the Microsoft Computer Dictionary, 5th Ed., incorporating the definition of "instruction" provided by the Dictionary of Computer and Internet Terms, 1st Ed., published August 2016. Examiners also agreed that the term "instruction," as it is used in the CPU definition, is defined in the Dictionary of Computer and Internet Terms, 1st Ed., published August 2016.[1]

Examiner's interpretation of the claim term "*processor*" and PO's latest interpretation of the claim term "*processor*" are presented in the table below.

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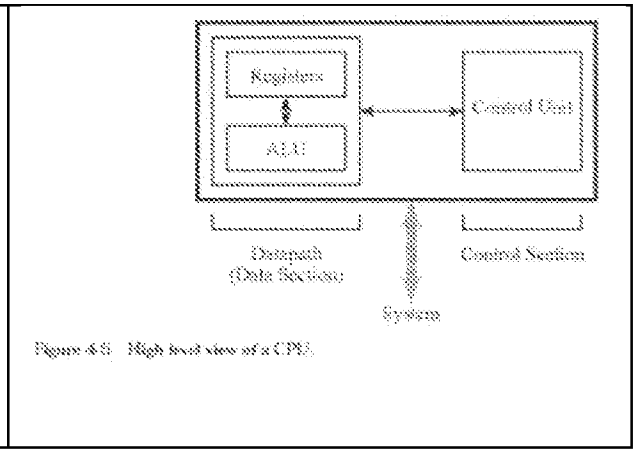
[1] Examiners note this definition is dated August 2016, which is after the effective filing date of the '444 Patent, which is January 15, 2014.

CLAIM INTERPRETATION (Ordinary and Customary)	
Examiners' Interpretation of "Processor"	**PO's Interpretation of "Processor"**
CPU n. Acronym for central processing unit. The computational and control unit of a computer. The CPU is the device that interprets and executes instructions. Mainframes and early minicomputers contained circuit boards full of integrated circuits that implemented the CPU. Single-chip central processing units, called *microprocessors*, made possible personal computers and workstations. Examples of single-chip CPUs are the Motorola 68000, 68020, and 68030 chips and the Intel 8080, 8086, 80286, 80386, and i486 chips. The CPU – or microprocessor, in the case of a microcomputer – has the ability to fetch, decode, and execute instructions and to transfer information and to and from other resources over the computer's main data-transfer path, the bus. By definition, the CPU is the chip that functions as the "brain" of a computer. In some instances, however, the term encompasses both the processor and the computer's memory or, even more broadly, the main computer console (as opposed to peripheral equipment), See the illustration. *See also* microprocessor. **Instruction** (n) – An action statement in any computer language, most often in machine or assembly language. Most programs consist of two types of statements: declarations and instructions.	**CPU** n. Acronym for central processing unit. The computational and control unit of a computer. The CPU is the device that interprets and executes instructions. Mainframes and early minicomputers contained circuit boards full of integrated circuits that implemented the CPU. Single-chip central processing units, called *microprocessors*, made possible personal computers and workstations. Examples of single-chip CPUs are the Motorola 68000, 68020, and 68030 chips and the Intel 8080, 8086, 80286, 80386, and i486 chips. The CPU – or microprocessor, in the case of a microcomputer – has the ability to fetch, decode, and execute instructions and to transfer information and to and from other resources over the computer's main data-transfer path, the bus. By definition, the CPU is the chip that functions as the "brain" of a computer. In some instances, however, the term encompasses both the processor and the computer's memory or, even more broadly, the main computer console (as opposed to peripheral equipment), See the illustration. *See also* microprocessor. **Instruction** (n) – An action statement in any computer language, most often in machine or assembly language. Most programs consist of two types of statements: declarations and instructions. "At a minimum, the CPU consists of a data section that contains registers and an ALU, and a control section, which interprets and effects register transfers, as illustrated in figure 4-5."



(1) PO argues figure 39 of Okamura is not a "*processor*" within the ordinary and customary meaning of the term because Okamura's figure 39 does not include registers, an ALU, and a control unit (see Remarks 7-10).

This argument is not persuasive because the ordinary and customary meaning of the term "*processor*" does not require registers, an ALU, and a control unit because Examiners maintain a "*processor*" does not require registers, an ALU, and a control unit.

(2) PO argues Okamura's synchronous separator circuit (fig. 39, #111) does not read on the claimed "*processor*" and cites Texas Instruments LM1881 Liquid Crystal Display Driver as providing an example of a typical synchronous separator and distinguishes this synchronous separator (i.e., the LM1881) from the claimed "*processor*" because the synchronous separator (i.e., the LM1881) does not contain registers, an ALU, nor a control circuit (see Remarks pgs. 8-9).

PO also cites Texas Instruments MM5483 Liquid Crystal Display Driver as providing an example of a typical synchronous separator and distinguishes this synchronous separator (i.e., the MM5483) from the claimed "*processor*" because the

synchronous separator (i.e., the MM5483) does not contain registers, an ALU, nor a control circuit (see Remarks pgs. 9-10)

Neither of these arguments are persuasive for two reasons. First, the anticipation rejection does not find that Okamura's synchronous separator circuit (fig. 39, #111) reads on the claimed "*processor*." Rather, the rejection states:

> Okamura necessarily discloses a "processor" because the pixel shifts of figure 36 are necessarily images processed by a computer. Specifically, it is well-known that a pixel is the smallest unit of a digital image. Because pixels are the basic logical unit in digital graphics, they are necessarily processed by a computer. (Final Action mailed April 19, 2024; pgs. 9-10)

Because the rejection never alleges Okamura's synchronous separator circuit (fig. 39) reads on the claimed "*processor,*" traversing this position does not traverse the rejection.

Second, the argument is not persuasive because the ordinary and customary meaning of the term "*processor*" does not require registers, an ALU, and a control unit because Examiners maintain a "*processor*" does not require registers, an ALU, and a control unit.

(3) PO argues that that the processor disclosed at figure 39 of Okamura has no ability to interpret and execute instructions and therefore cannot fall within the scope of the ordinary and customary meaning of the claim term "*processor*" because "sampling control circuit (#117) is a delicate [sic] control circuit to control liquid control circuit (#118), it includes combinational circuits and sequential circuits which can generate timing sequence signals to control (instruct) liquid control circuit, which means the sampling control circuit (#117) can generate a delicate [sic] instruction to instruct liquid control circuit (#118), but the sampling control circuit (#117) cannot receive different

instructions from memory of a computer and interprets the instructions and executes different instructions just like the control unit of a processor which is a universal controller to perform kinds of different operations based on program instruction stored in the main memory of a computer" (see Remarks pgs. 10-11).

As best understood, this argument is not persuasive because PO acknowledges that the sampling timing signals and the control signals of sampling control circuit (#117L) of figure 39 are instructions in that they instruct the liquid control circuit (#118L) and the switch circuit (#114R) (see Okamura; col.24:4-23). As such, Examiners maintain that figure 39 of Okamura reads on the claimed "*processor*" because the ordinary and customary meaning of the claim term "*processor*" requires a device that interprets and executes instructions and the sampling timing signals and the control signals of sampling control circuit (#117L) are instructions in that they instruct the liquid control circuit (#118L) and the switch circuit (#114R) (see col.24:4-23). (see Claim interpretation section above).

(4) PO argues the Microsoft Computer Dictionary definition's statement that "[m]ainframes and early minicomputers contained circuit boards full of integrated circuits that implemented the CPU" actually means "early minicomputers include a plurality of circuit boards and not integrated into a single chip." (see Remarks 11). PO cites a blog post, without a publication date, titled "*Microprocessor vs. Integrated Circuit—What's the difference*," where it can be reasonably inferred that the earliest possible date is 2019 because it refers to the AMD Epyc Rome, is which cited as being released in 2019.

This argument is not persuasive for at least two reasons. First, the article pertains to microprocessors, which is not claimed. Rather, "*processors*" are claimed. Second, PO relies on a blog post dated no earlier than 2019 to redefine early minicomputers by stating that a statement in the Microsoft Computer Dictionary ("the Dictionary") actually means something wholly different. The Dictionary states "[m]ainframes and early minicomputers contained circuit boards full of integrated circuits that implemented the CPU. Single-chip central processing units, called *microprocessors*, made possible personal computers and workstations." Nowhere does the Dictionary state that integrated circuits are microprocessors. And, redefining early microcomputers as such is merely a red herring because whether a microprocessor is an integrated circuit is not at issue in this proceeding.

(5) PO argues Okamura's circuit structure disclosed at figure 39 is not a "*processor*" and as such, the pixel shifts of figure 36 are not necessarily images processed by a computer (see Remarks 14-15).

This argument is not persuasive because it is premised on a finding that Okamura's figure 39 is not a "*processor*" within the ordinary and customary meaning of the term, which Examiners reject.

Because Examiners maintain Okamura necessarily discloses a "*processor*" because the pixel shifts of figure 36 are necessarily images processed by a computer

and PO's arguments are directed to figure 39, which is not the basis of the rejection,

PO's arguments are not persuasive.

Signed:

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Reexamination Specialist, Art Unit 3992

Conferees:

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Primary Examiner, Art Unit 3991
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Supervisory Patent Examiner, Art Unit 3992